

In re Patent Application of:
ZENG
Serial No. 09/844,347
Filing Date: April 27, 2001

the gate conducting layer 24. The MOSFET 70 is advantageously formed with a reduced on-resistance without degrading device ruggedness. The on-resistance is reduced since the source/body contact regions 82 are laterally spaced apart from the gate conducting layer 24. The source/body contact regions 82 thus provide an efficient short between the source and body regions of the MOSFET 70. As a result, device ruggedness is increased. --

In the Claims:

Please amend the claims as follows:

Please cancel Claims 1-22 without prejudice to Applicant's right to file a divisional application directed to the subject matter thereof.

sub B1
X5

23. (Amended) A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining the trench;
a gate conducting layer in a lower portion of the trench;
a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;
source regions adjacent the outwardly extending dielectric layer; and
source/body contact regions laterally spaced apart from said gate conducting layer.

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*AS
end*

24. (Amended) A MOSFET according to Claim 23,
further comprising a source electrode on said source regions
and on said dielectric layer.

Please add new Claims 32 - 39.

*sub
of*

Rule 1.126

Ab

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21. A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining the trench;
a gate conducting layer in a lower portion of the
trench;
a dielectric layer in an upper portion of the trench
and extending outwardly from said semiconductor layer;
source regions adjacent the outwardly extending
dielectric layer;
source/body contact regions laterally spaced from
said gate conducting layer and non-interruptibly contacting
said source regions;
at least one conductive via between said source
electrode and said source/body contact regions; and
a source electrode on said source regions, on said
dielectric layer and on said at least conductive via.

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32. A MOSFET according to Claim 31, wherein a
portion of said source regions include a recess over said
source/body contact regions.

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33. A MOSFET according to Claim 31, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.

35
34. A MOSFET according to Claim 31, wherein said gate conducting layer is recessed in the trench within a range of about 0.2 to 0.8 microns from an opening thereof.

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35. A MOSFET comprising:
a semiconductor layer having a trench therein;
a gate dielectric layer lining the trench;
a gate conducting layer in a lower portion of the trench;
a dielectric layer in an upper portion of the trench and extending outwardly from said semiconductor layer;
source regions adjacent the outwardly extending dielectric layer and including an opening therein; and
source/body contact regions laterally spaced from said gate conducting layer and non-interruptibly contacting said source regions, said source/body contact regions being exposed by the opening in said source regions.

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36. A MOSFET according to Claim 35, further comprising a source electrode on said source regions, on said dielectric layer, and on said source/body contact regions.

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37. A MOSFET according to Claim 35, wherein said outwardly extending dielectric layer extends from said source regions equal to or less than about 1 micron.